AMENDMENTS TO THE CLAIMS

1-10 (Canceled).

11. (New) A semiconductor device comprising:

N stages of delay cells, each of the N delay cells delaying an input clock signal by 1/N clock period and outputting the respective delayed clock signal;

a reference signal phase detection circuit for detecting a phase state of a present reference signal based on phase differences between the clocks outputted from the delay cells and the present reference signal, and detecting a phase state of a previous reference signal based on phase differences between the clocks outputted from the delay cells and the previous reference signal;

a comparison circuit for comparing the phase state of the present reference signal and the phase state of the previous reference signal which are detected by the reference signal phase detection circuit;

a phase control circuit for shifting the phase state of the present reference signal to make it coincide with the phase state of the previous reference signal, when the comparison circuit detects that the phase states of the present reference signal and the previous reference signal do not coincide with each other;

a selector; and

a selector control circuit for controlling the selector based on the output of the phase control circuit to select a clock which is most synchronized with the shifted phase state of the present reference signal from among clocks outputted from the respective delay cells, and to output the selected clock as a sync clock,

12. (New) A semiconductor device as defined in Claim 11 wherein said phase control circuit performs the phase control by counting up the number of clocks stepwisely.

13. (New) A semiconductor device as defined in Claim 11 wherein said phase control circuit performs the phase control by counting down the number of clocks stepwisely.

14. (New) A semiconductor device as defined in Claim 11 wherein said phase control circuit shifts the phase of the clock of the present reference signal at a clock rate interval equivalent to a (1+N)/N clock so as to bring the phase of the present reference signal close to the phase of the previous reference signal.

15. (New) A semiconductor device as defined in Claim 11 wherein said phase control circuit shifts the phase of the clock of the present reference signal at a clock rate interval equivalent to a (N-1)/N clock so as to bring the phase of the present reference signal close to the phase of the previous reference signal.

16. (New) A semiconductor device as defined in Claim 11 wherein said phase control circuit shifts the phase of the clock of the present reference signal so that the clock rate interval becomes equal to or larger than one clock to bring the phase of the present reference signal close to the phase of the previous reference signal.

17. (New) A semiconductor device as defined in Claim 11 wherein said phase control circuit shifts the phase of the clock of the present reference signal so that the clock rate interval becomes equal to or smaller than one clock to bring the phase of the present reference signal close to the phase of the previous reference signal.

18. (New) A semiconductor device as defined in Claim 11 wherein said phase control circuit counts the number of clocks clock by clock, and performs the phase control on the basis of the count value.

19. (New) A semiconductor device as defined in Claim 11 wherein said phase control circuit counts the number of clocks in units of 1/M-lines, wherein M is an integer not less than 2, and performs the phase control on the basis of the count value.

20. (New) A semiconductor device as defined in Claim 11 wherein said phase control circuit counts the number of clocks line by line, and performs the phase control on the basis of the count value.